XILINX | UNIVERSITY PROGRAM

CoreEL Technologies
Enabling Excellence

System Design Flow on Zynq using Vivado

Course Description	This course provides professors necessary skills to design and debug a system using Vivado IP Integrator, hardware analyzer, and Vitis.
Duration	2 Days
Who should attend?	Professors who are familiar with Xilinx programmable technology and wish to get up to speed with SoC-based system design using Zynq.
Pre-requisites	• Digital logic and FPGA design experience • Basic experience with Xilinx Vivado design software suite • Basic understanding of C programming

Course Overview

Day 1:

- 7-Series Architecture Overview
- Vivado Design Flow
- **Lab 1: Creating an HDL Design**
    - Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL simulator available in Vivado design suite. Generate the bitstream and verify in hardware.
- Xilinx Design Constraints
- **Lab 2: Xilinx Design Constraints**
    - Create a project with I/O Planning type, enter pin locations, and export it to the rtl. Then create the timing constraints and perform the timing analysis.
- IP Integrator and Embedded System Design Flow
- **Lab 3: Create a Processor System using IP Integrator**
    - Create a simple ARM Cortex-A9 based processor design targeting the Pynq Z2 Board using IP Integrator.

Day 2:

- Embedded System Design with Custom IP
- **Lab 4: Creating and Adding Your Own Custom IP**
    - Use the Manage IP feature of Vivado to create a custom IP and extend the system with the custom peripheral. Write a basic C application to access the peripherals.
- System Debugging using Vivado Logic Analyzer and Vitis
- **Lab 5: Debugging using Vivado Logic Analyzer cores**
    - Insert various Vivado Logic Analyzer cores to debug/analyze system behaviour.