09.06.2025 to 13.06.2025

Workshop on "Device Modeling and Circuit Simulation for Integrated Circuit Designs"

(UNDER THE ANCHOR INSTITUTE PROGRAM)

Anchor Institute Programme Office
Dhirubhai Ambani University (formerly DA-IICT),
GANDHINAGAR,GUJARAT

- **Supported by:** The Centre for Entrepreneurship Development (CED)-A Government of Gujarat Organization funded Anchor Institute DA-IICT.

- **Organized by:** Dhirubhai Ambani University (formerly DA-IICT), Gandhinagar, Gujarat, India.

Workshop Start Date	09.06.2025 to 13.06.2025
Venue	Dhirubhai Ambani University (formerly DA-IICT)
Program Schedule	Click here
Course Duration	The duration of the course will be 40 hours, consisting of 20 hours of theory sessions and 20 hours of laboratory sessions.
Target Audience	Professionals, Faculties, Ph.D. Scholar, PG and Final year UG Students
Course Fee (Pay Online)	Participants from Gujarat state are charged a fully refundable upfront course fee of 5,000 INR. Please note that this fee is non-refundable for candidates from other states. ***Please note that the registration fee will not be collected at the time of registration. A separate Google Form link for fee payment will be shared with shortlisted candidates after the scrutiny of all received applications.***
Accommodation	Complimentary accommodation, tea/coffee, and lunch will be provided throughout the workshop.
Refund Policy	Maintain a 75% minimum attendance to be eligible for the refund.
Certificate	A participation certificate will be conferred to individuals who maintain an attendance record of at least 75%.

- **Registration on the following link after the payment:**

To enroll, please complete the registration form by clicking here. Once you open the registration form, you will find further instructions and details.

The last day of registration is **1st June. 2025**

1. Course Objective

The course aims at delivering the fundamentals of electronic devices comprising BJTs and MOSFETs for realization of different digital as well as analog circuits and system design. The circuit simulation using SPICE will be imparted. The basics of SPICE commands, varying analyses, circuit level schematic realization, netlist extraction and layout based design implementation will be extensively focused. The device analytical formulation using MATLAB and its correlation with SPICE simulative platform will be detailed. The modeling and simulation of next-generation, futuristic and upcoming nanotechnology based graphene derived FETs and interconnects for integrated circuits will also be discussed.
The main purpose of this course is to impart professional training so as to meet the current state-of-the-art requirements of Electronics and VLSI industry. To attain all these specific goals, lectures followed by extensively lab exercises on different electronic design and automation tools will be provided.

2. Expected Outcome

- The participants shall be able to design and analyze circuits for different applications. This shall facilitate the participants to design and execute research projects and meet industrial needs.
- Prominently able to understand and attain hands on training of simulative modeling, analytical formulation and their correlation with each other.
- Able to understand process design flow for VLSI system design for integrated circuits.

3. Organizers and Course Instructors:

Dr. Rutu Parekh did her M. Eng. in Electrical Engineering from Concordia University, Montreal, Canada, PhD in Electrical Engineering (Nanoelectronics) from Université de Sherbrooke, Sherbrooke, Canada and as a Postdoctoral fellow at Centre of Excellence in Nanoelectronics, IIT Bombay in 2015. Her research areas are Micro / Nano electronics, Nanofabrication, embedded systems and IOE. She has research experience with École Polytechnique de Montréal, industrial experience with eInfochips, Ahmedabad, India and HP Karkland, Montreal, and teaching experience with Nirma University of Science and Technology, Ahmedabad. She is currently working as an Associate Professor at DA-IICT, Gandhinagar, India. In addition, she has been offering service as a Visiting Associate with The Inter-University Centre for Astronomy and Astrophysics, Pune, India, and also as technical advisor and a Board member of the committees. She has been actively engaged in sponsored research and development projects in the area of embedded systems, ASIC design related to military and space applications. She has published book and a number of international journal and conference articles related to her research areas. She is founder and chair of IEEE NTC chapter.

Dr. Yash Agrawal is faculty at Dhirubhai Ambani University (formerly DA-IICT). His specialization includes VLSI, Nanotechnology, AI/Models for VLSI, Numerical Method Techniques--FDTD, device modulation and simulation, design techniques and modelling schemes of high-speed on-chip VLSI interconnects, Network-on-chip designs, flexible electronics, VLSI design for bio-medical applications, image processing using FPGA. He did his Postdoc from University of Rennes, France. He received his Ph.D. and M.Tech. Degrees in VLSI Design Automation and Techniques from NIT, Hamirpur, Himachal Pradesh, India. Dr. Yash has been expert and distinguished guest at various places. He has several publications in Book Chapters of Springer, IGI, Journals including IEEE Transactions in Electromagnetic Compatibility, IEEE Transactions in Nanotechnology, Springer, Taylor and Francis and several national and international reputed Conferences. He is guiding several Ph.D. and M.Tech. students. He is chair of both IEEE Electron Devices and Solid State Circuit societies, Gujarat section, India.

4. Address for Correspondence:

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