16.06.2025 to 20.06.2025

# *Workshop on "Speech and Audio Signal Processing using FPGA"*

**(UNDER THE ANCHOR INSTITUTE PROGRAM)**

Anchor Institute Programme Office
Dhirubhai Ambani University (formerly DA-IICT),
GANDHINAGAR,GUJARAT

- **Supported by:** The Centre for Entrepreneurship Development (CED)-A Government of Gujarat Organization funded Anchor Institute Dhirubhai Ambani University (formerly DA-IICT).
- **Organized by:** Dhirubhai Ambani University (formerly DA-IICT), Gandhinagar, Gujarat, India.

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| **Workshop Start Date** | 16.06.2025 to 20.06.2025 |
| **Venue** | Dhirubhai Ambani University (formerly DA-IICT) |
| **Program Schedule** | Click here |
| **Course Duration** | The duration of the course will be 40 hours, consisting of 20 hours of theory sessions and 20 hours of laboratory sessions. |
| **Target Audience** | Professionals, Faculties, Ph.D. Scholar, PG and Final year UG Students |
| **Course Fee (Pay Online)** | Participants from Gujarat state are charged a fully refundable upfront course fee of 5,000 INR. Please note that this fee is non-refundable for candidates from other states. ***Please note that the registration fee will not be collected at the time of registration. A separate Google Form link for fee payment will be shared with shortlisted candidates after the scrutiny of all received applications.*** |
| **Accommodation** | Complimentary accommodation, tea/coffee, and lunch will be provided throughout the workshop. |
| **Refund Policy** | Maintain a 75% minimum attendance to be eligible for the refund. |
| **Certificate** | A participation certificate will be conferred to individuals who maintain an attendance record of at least 75%. |

- **Registration on the following link after the payment:**

To enroll, please complete the registration form by clicking here. Once you open the registration form, you will find further instructions and details.

The last day of registration is **8th June. 2025**

## 1. Course Objective

The objective of the course is to provide students with a comprehensive understanding of fundamental algorithms in speech and audio processing, and corresponding hardware accelerators and its implementation using FPGA.

The key algorithms covered includes convolution, hardware elements (adder, delay, and multiplier) to implement difference equation, 2nd order digital resonators (biquad circuits), Fast Fourier Transform (FFT) architectures, spectrogram, design of sigma-delta ADC, sample and hold circuits, etc.

The course focuses on fundamentals and hands-on training on MATLAB/Python, Verilog HDL, and FPGA.

## 2. Expected Outcome

Upon completing the Speech and Audio Processing using FPGA course, participants can expect to achieve the following outcomes:

- Basic understanding of Audio/Speech Processing.
- Hardware Description Language (HDL) – Verilog for FPGA based Embedded System Boards.
- Hands-on-training of FPGA boards, with exposure to MATLAB, Python, Verilog platforms.
- Hardware Accelerators and Neural-Network conceptualization for Audio/Speech processing.
- Exposure to various applications and real-time project development.

## 3. Organizers and Course Instructors:

**Dr. Yash Agrawal** is faculty at Dhirubhai Ambani University (formerly DA-IICT). His specialization includes VLSI, Nanotechnology, AI/Models for VLSI, Numerical Method Techniques--FDTD, device modulation and simulation, design techniques and modelling schemes of high-speed on-chip VLSI interconnects, Network-on-chip designs, flexible electronics, VLSI design for bio-medical applications, image processing using FPGA. He did his Postdoc from University of Rennes, France. He received his Ph.D. and M.Tech. Degrees in VLSI Design Automation and Techniques from NIT, Hamirpur, Himachal Pradesh, India. Dr. Yash has been expert and distinguished guest at various places. He has several publications in Book Chapters of Springer, IGI, Journals including IEEE Transactions in Electromagnetic Compatibility, IEEE Transactions in Nanotechnology, Springer, Taylor and Francis and several national and international reputed Conferences. He is guiding several Ph.D. and M.Tech. students. He is chair of both IEEE Electron Devices and Solid State Circuit societies, Gujarat section, India.

**Dr. Hemant A. Patil** received Ph.D. degree from the Indian Institute of Technology (IIT), Kharagpur, India, in July 2006. Since 2007, he has been a faculty member at Dhirubhai Ambani University (formerly DA-IICT), and developed Speech Research Lab at Dhirubhai Ambani University (formerly DA-IICT), which is recognized as ISCA speech labs. Dr. Patil is member of IEEE, IEEE Signal Processing Society, IEEE Circuits and Systems Society, International Speech Communication Association (ISCA), EURASIP and an affiliate member of IEEE SLTC. He is regular reviewer for ICASSP and INTERSPEECH, Speech Communication, Elsevier, Computer Speech and Language, Elsevier and Int. J. Speech Tech, Springer, Circuits, Systems and Signal Processing, Springer. He has published around 226 research publications in national and international conferences/journals/book chapters. He visited department of ECE, University of Minnesota, Minneapolis, USA (May-July, 2009) as short term scholar. He has been associated (as PI) with three MeitY sponsored projects in ASR, TTS and QbE-STD. He was co-PI for DST sponsored project on India-Digital Heritage (IDH)-Hampi. His research interests include speech and speaker recognition, TTS, infant cry analysis. He has received DST Fast Track Award for Young Scientists for infant cry analysis. He has coedited a book on Forensic Speaker Recognition with Dr. Amy Neustein (EIC, IJST Springer). Presently, he is coediting two books in speech technology for medical-domain.

## 4. Address for Correspondence:

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